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GRAY VOLTAGE GENERATION CIRCUIT FOR DRIVING A LIQUID CRYSTAL DISPLAY RAPIDLY

Field of the Invention

The present invention relates to a liquid crystal display and, more particularly, to a gray voltage generation circuit for driving a liquid crystal display and such a liquid crystal display.

Background of the Invention

Generally, a liquid crystal is an organic compound having a neutral property between liquid and crystal, and changes in its color or transparency by voltage or temperature. A liquid crystal display (LCD), which expresses information using the liquid crystal, occupies a smaller volume and has a lower power consumption than a conventional display device. Therefore, lots of attentions are paid to the LCD as a novel display device.

Fig. 1 schematically illustrates a configuration of a conventional liquid crystal display. A liquid crystal display 10 includes a liquid crystal panel 1, a gate driving circuit 2 coupled to the liquid crystal panel 1, a source driving circuit 3, a timing control circuit 4, and a gray voltage generation circuit (or gamma reference voltage generation circuit) 5.

The liquid crystal panel 1 is made of a plurality of gate lines G0 through Gn and a plurality of data lines D1 through Dm that are vertically interconnected with the gate lines, respectively. The gate driving circuit 2 is connected to each of the gate lines G0 through Gn, and the source driving circuit 3 is connected to each of the data lines D1

through Dm. One pixel is composed in each interconnection of the gate lines and the data lines. Each pixel is made of one thin film transistor (TFT), one storing capacitor Cst, and one liquid crystal capacitor Cp. Each of pixels composing the liquid crystal panel 1 further includes three sub-pixels corresponding to red (R), green (G), and blue (B). A pixel displayed via the liquid crystal panel 1 is obtained by combination of R, G, and B color filters. The liquid crystal display 10 can display not only color pictures but also pure red, green, blue, and gray scales by combining those pixels.

The timing control circuit 4 issues control signals (e.g., gate clock and gate on signals) required in the gate driving circuit 2 and the source driving circuit 3 in response to color signals R, G, and B, horizontal and vertical synch signals HSync and Vsync, and a clock signal CLK. The gray voltage generation circuit 5 is connected to the source driving circuit 3, generating a gray voltage Vgray or a gamma reference voltage that is a reference to generate a liquid crystal driving voltage Vdrive. One example of the gray voltage generation circuit 5 is disclosed in U. S. Patent No. 6,067,063 entitled "LIQUID CRYSTAL DISPLAY HAVING A WIDE VIEW ANGLE AND METHOD FOR DRIVING THE SAME", issued to Kim *et al.*, issued on May 23, 2000. A gray voltage generation circuit 5 disclosed therein includes a plurality of resisters R1 through Rn+1 that are directly coupled between a power supply voltage (Vcc) and a ground (GND). Each of the resisters R1 through Rn+1 distributes the power supply voltage (Vcc) with a predetermined ratio, generating n-bit gray voltages VG1 through VGn.

Now, operations of the liquid crystal display 10 having such a configuration will be described in detail. If the gate driving circuit 2 sequentially scans pixels of the panel row by row, the source driving circuit 3 generates a liquid crystal driving voltage Vdrive

based upon the color signals R, G, and B inputted through the timing control circuit 4, in response to the reference voltage Vgray outputted from the gray voltage generation circuit 5. And then, the source drive 3 applies the generated voltage Vdrive to the panel 1 each time of scanning.

In such an operation, the TFT acts as a switch. For example, when the TFT is turned on, the liquid crystal capacitor Cp is charged by the liquid crystal driving voltage Vdrive generated from the source driving circuit 3. When the TFT is turned off, the capacitor Cp prevents the charged voltage from leaking. This shows that the liquid crystal driving voltage Vdrive applied from the source driving circuit 3 has a great influence upon driving each TFT composing the panel 1.

As the liquid crystal display tends to implement high speed response, it is required to enhance a response speed of such a liquid crystal display Cp in order to speed up the device. This is because if the voltage Vdrive applied from the source driving circuit 3 has a high value, the capacitor Cp would quickly be charged to enhance a total driving speed of a liquid crystal display.

There are many methods of boosting a liquid crystal driving voltage Vdrive applied from the source driving circuit 3 in order to enhance a driving speed of the liquid crystal display. For example, it requires a design change of the gate driving circuit 2 or the source driving circuit to generate a liquid crystal driving voltage Vdrive of high level, or a design change of the timing control circuit 4 for issuing a control signal to the driving circuits 2 and 3. Unfortunately, changing designs of such high-priced circuits causes higher costs in a production unit. Furthermore, the increased liquid crystal driving voltage Vdrive also increases power consumption of the liquid crystal display in

proportion to the voltage Vdrive rise.

Accordingly, the object of the present invention is to overcome the foregoing drawbacks, and to provide a gray voltage generation circuit that can enhance a driving speed of a liquid crystal display with low cost and power consumption.

Summary of the Invention

To attain this object, there is provided a liquid crystal display that includes a liquid crystal panel having a plurality of pixels, a gray voltage generation circuit for generating a plurality of gray voltages corresponding to data to be displayed in the liquid crystal panel, a timing control circuit for issuing a gate clock signal and a plurality of control signals, a gate driving circuit for sequentially scanning the pixels row by row in response to the gate clock signal, and a source driving circuit for generating a liquid crystal driving voltage in response to the data and applying the generated liquid crystal driving voltage to the panel each time of scanning. In response to the gray voltage, the source driving circuit generates a liquid crystal driving voltage that has different values in high and low level intervals.

Brief Description of the Drawings

Fig. 1 is a block diagram showing a configuration of a conventional liquid crystal display.

Fig. 2 is a block diagram showing a configuration of a liquid crystal display in accordance with the present invention.

Fig. 3 is a block diagram showing a configuration of a gray voltage generation circuit in accordance with the present invention.

Fig. 4 is a circuit diagram showing a detailed configuration of a clock generator

shown in Fig. 3.

Fig. 5 is a circuit diagram showing a detailed configuration of a voltage generator shown in Fig. 3.

Fig. 6 is a circuit diagram showing a detailed configuration of a gray voltage generation circuit shown in Fig. 3.

Figs. 7A and 7B are waveform diagrams showing one example of waveforms of gray voltages that are generated from a gray voltage generation circuit in accordance with the present invention.

Figs. 8 and 9 are waveform diagrams showing one example of waveforms of outputs of a source driving circuit, which are generated by applying the gray voltage shown in Figs. 7A and 7B.

Figs. 10A, 10B, 11A, 11B, 12A, 12B, 13A and 13B are timing diagrams showing response speed measuring results of 0-32, 0-48, 0-64, and 32-84 grays of the source driving circuits by means of the gray voltage shown in Figs. 7A and 7B.

Description of the Preferred Embodiment

A new and improved gray voltage generation circuit of a liquid crystal display is provided to the present invention. The gray voltage generation circuit generates a high-potential liquid crystal driving voltage for a predetermined interval so that liquid crystal capacitors may be charged in a short time, and alters and outputs a gray voltage after the predetermined interval in order to generate a normal liquid crystal driving voltage. As a result, a driving speed of the liquid crystal display can be enhanced.

Fig. 2 schematically illustrates a configuration of a liquid crystal display 100 according to the present invention. The liquid crystal display 100 includes a liquid

display panel 1, a plurality of gate driving circuits 2 coupled to the panel 1, a plurality of source driving circuits 3, a timing control circuit 4, and a gray voltage generation circuit 50. Such a configuration is identical to the configuration of the conventional liquid crystal display shown in Fig. 1, except for a gray voltage generation circuit 50 for generating a gray voltage Vgray' in response to a gate clock signal Gate Clock issued from a timing control circuit. Same numerals denote same elements throughout the drawings, and their description will be skipped herein so as to avoid duplicate description.

It is well known that the source driving circuit 3 selects one of a plurality of gray voltages according to color signals (R, G, and B), and applies a liquid crystal driving voltage Vdrive to a liquid crystal panel in response to the selected one gray voltage. A function of the source driving circuit 3 is closely bound up with a charging speed of the liquid crystal display Cp constructed in the liquid crystal panel 1. The liquid crystal driving voltage Vdrive is dependent upon the gray voltage Vgray' generated from the gray voltage generation circuit 50. Therefore, a liquid crystal display 100 of the invention changes a liquid crystal driving voltage Vdrive generated from the source driving circuit 3 so as to enhance a charging speed of the liquid crystal capacitor Cp constructed in the panel 1. Without modifying designs of expensive and complex circuits such as the gate driving circuit 2, the source driving circuit 3, and the timing control circuit 4, a gray voltage generation circuit 50 of much lower price than the above circuits is made to enhance a driving speed of the liquid crystal display 100.

Fig. 3 schematically illustrates a configuration of a gray voltage generation circuit according to the present invention. A gray voltage generation circuit 50 includes a clock generator 52, a voltage generator 54, and a gray voltage generator 56. The

clock generator 52 generates n-bit clock signals G_CLK1, ..., and G_CLKn that are not overlapped with each other, in response to a gate clock signal GATE CLOCK. The voltage generator 54 generates n-bit reference voltages Vref1, ..., and Vrefn each having different level, in response to a power supply voltage V_{DD} that is an analog signal and is used as a power supply voltage of a source driving circuit 3.

If the n-bit clock signals G_CLK1, ..., and G_CLKn and the n-bit reference voltages Vref1, ..., and Vrefn are inputted to the gray voltage generator 56, the gray voltage generator 56 generates m-bit gray voltages Vgray1', ..., and Vgraym' that are synchronized with the clock signals G_CLK1, ..., and G_CLKn to have different potentials based upon levels of the reference voltages Vref1, ..., and Vrefn. Although described in detail hereinbelow, the gray voltages Vgray1', ..., and Vgraym' makes the source driving circuit 3 generate a liquid crystal driving voltage Vdrive' that has different values in high and low intervals of the clock signal CLOCK during one period of the gate clock GATE CLCK. The liquid driving voltage Vdrive' of the source driving circuit 3 having such a characteristic can enhance a driving speed of a liquid crystal display 100.

Figs. 4, 5 and 6 illustrate the clock generator 52, the voltage generator 54, and the gray voltage generator 56 that are shown in Fig. 3, respectively. The clock generator 52 issues six clock signals C_CLK1, ..., and C_CLK6. The voltage generator 54 generates six reference voltages Vref1, ..., and Vref6. And, the gray voltage generator 56 generates ten clock signals G_CLK1', ..., and G_CLK10' in response to the six clock signals C_CLK1, ..., and C_CLK6 and the six reference voltages Vref1, ..., and Vref6. According to a circuit configuration, the number of generated signals can be changed. The circuits shown in the drawings are merely one example of the circuit

configuration.

Referring now to Fig. 4, the clock generator 52 consists of an input terminal for receiving a gate clock signal GATE CLOCK generated from the timing control circuit 4, first and sixth clock generation units 52a-52f each being coupled to the input terminal in parallel, and first and sixth output terminals each being coupled to the units 52a-52f. Each of the units 52a-52f has a capacitor C1, ..., or C6 and a resister R1, ..., or R6 that are serially connected between the input terminal and the output terminal. And, each of the units 52a-52f outputs first and sixth clock signals G_CLK1, ..., and G_CLK6 not to be overlapped with each other. A period of the clock signals G_CLK1, ..., and G_CLK6 is identical to that of the gate clock signal GATE CLOCK generated from the timing control circuit 4.

Referring to Fig. 5, the voltage generator 54 consists of six voltage generation units 54a-54f for generating six reference voltages Vref1, ..., and Vref6 by dividing a power supply voltage V_{DD} at a predetermined ratio to generate six reference voltages of different levels. The units 54a-54f are connected between the power supply voltage V_{DD} and a ground voltage GND in parallel. Each of the units 54a-54f includes two resisters serially connected between VDD and GND, and an output terminal coupled to a contact point between the resisters.

Referring to Fig. 6, the gray voltage generator 56 consists of first and second gray voltage generation units 56a and 56b. The first gray voltage unit 56a generates first to fifth gray voltages Vgray1', ..., and Vgray5' that are used to drive a positive polarity of a liquid crystal. The second gray voltage unit 56b generates sixth to tenth gray voltages Vgray6', ..., and Vgray10' that are used to drive a negative polarity of a

liquid crystal.

The first gray voltage unit 56a includes first to sixth input terminals for receiving clock signals G_CLK1, G_CLK4, and G_CLK5 generated from a clock generator 52 and reference voltages Vref1, Vref4, and Vref5 generated from a voltage generator 54. It also includes a first amplifier AMP1, a second amplifier AMP2 and a third amplifier AMP3 for respectively adding and amplifying G_CLK1, G_CLK4, and G_CLK5 to a predetermined ratio to generate gray voltages Vgray1', Vgray4', and Vgray5', and output terminals for outputting Vgray1', Vgray4', and Vgray5'. The first amplifier circuit AMP1 adds G_CLK1 to Vref1, and amplifies it to a predetermined ratio to generate Vgray1'. The second amplifier circuit AMP2 adds G_CLK4 to Vref4, and amplifies it to a predetermined ratio to generate Vgray4'. And, the third amplifier circuit AMP3 adds G_CLK5 to Vref5, and amplifies it to a predetermined ratio to generate Vgray5'.

The gray voltages Vgray1', Vgray4', and Vgray5' are given by the following equations;

<Equation 1>

$$Vgray1' = \frac{R19 + R20}{R19}\left[Vref1 + \frac{R1}{R1 + R19} V_{G\_CLK1}\right]$$

<Equation 2>

$$Vgray4' = \frac{R25 + R26}{R25}\left[Vref4 + \frac{R4}{R4 + R25} V_{G\_CLK4}\right]$$

<Equation 3>

$$Vgray5' = \frac{R27 + R28}{R27}\left[Vref5 + \frac{R5}{R5 + R27} V_{G\_CLK5}\right]$$

wherein V_{G_CLKn} represents an alternative element of a gate clock signal GATE CLOCK.

The first gray voltage generation unit 56a generates second and third gray voltages Vgray2' and Vgray3', as well as Vgray1', Vgray4', and Vgray5'. These gray voltages Vgray2' and Vgray3' have the level of a voltage that is divided by resisters R31, R32, and R33 that are serially connected between output terminals of the first and second amplifier circuit AMP1 and AMP2.

The second gray voltage generation unit 56b includes seventh to twelfth input terminals for receiving clock signals G_CLK2, G_CLK3, and G_CLK6 generated from the clock generator 52 and reference voltages Vref2, Vref3, and Vref6 generated from the voltage generator 54. It also has a fourth amplifier AMP4, a fifth amplifier AMP5, and a sixth amplifier AMP6 for subtracting G_CLK2, G_CLK3, and G_CLK6 from Vref2, Vref3, and Vref6 to generate gray voltages Vgray6', Vgray8', and Vgray10', and output terminals for outputting Vgray6', Vgray8', and Vgray10' generated from AMP4, AMP5 and AMP6. The fourth amplifier circuit AMP4 subtracts G_CLK2 from Vref2, and amplifies it to a predetermined ratio to generate Vgray6'. The fifth amplifier circuit AMP5 subtracts G_CLK3 from Vref3, and amplifies it to a predetermined ratio to generate Vgray8'. And, the sixth amplifier circuit AMP6 subtracts G_CLK6 from Vref6, and amplifies it to a predetermined ratio to generate Vgray10'.

The gray voltages Vgray6', Vgray8', and Vgray10' are given by the following equations;

<Equation 4>

$$Vgray6' = \frac{R2+R21+R22}{R22}\left[Vref2 - \frac{R22}{R2+R21} V_{G\_CLK2}\right]$$

<Equation 5>

$$Vgray8' = \frac{R3+R2+R24}{R24}[Vref3 - \frac{R24}{R3+R23} V_{G\_CLK3}]$$

<Equation 6>

$$Vgray10' = \frac{R6+R29+R30}{R30}[Vref6 - \frac{R30}{R6+R29} V_{G\_CLK6}]$$

wherein V_{G_CLKn} represents an alternative element of the gate clock signal GATE CLOCK.

The second gray voltage generation unit 56b generates eighth and ninth gray voltages Vgray8' and Vgray9', as well as Vgray6', Vgray7', and Vgray10'. These gray voltages Vgray8' and Vgray9' have the level of a voltage that is divided by resisters R38, R39, and R40 that are serially connected between output terminals of the fifth and the sixth amplifier circuit AMP5 and AMP6.

In the drawings, the fourth and seventh gray voltages Vgray4' and Vgray7' can be outputted through one or two terminals. For example, the fourth gray voltage Vgray4' generated through a fourth output terminal indicates that it uses an output of the second amplifier circuit AMP2 naturally. And, the fourth gray voltage Vgray4' generated through a fifth output terminal indicates that it divides the output of the second amplifier circuit AMP2 through a resister to a predetermined ratio for output. Based upon a circuit configuration, the gray voltages Vgray1', ..., and Vgray10' generated from the gray voltage generator 56 may use an output of an amplifier circuit naturally, or may divide and use the output of the amplifier circuit to a predetermined rate. Although Vgray4' and Vgray7' are illustrated in the drawing, they are simply examples. This can be

applied to any other gray voltages.

Figs. 7A and 7B exemplarily illustrate waveforms of gray voltages generated from a gray voltage generation according to the present invention. In particular, Fig. 7A shows a waveform of a gray voltage of a positive polarity, and Fig. 7B shows a waveform of a gray voltage of a negative polarity. Waveforms ① and ①', ② and ②', and ③ and ③' denote a gate clock signal GATE CLOCK issued from a timing control circuit 4, a 48-gray voltage, and a 64-gray voltage, respectively.

Figs. 8 and 9 exemplarily illustrate waveforms of outputs of a source driving circuit, which are generated by applying the gray voltage shown in Figs. 7A and 7B. In particular, Fig. 8 shows a waveform in driving dot inversion, and Fig. 9 shows a waveform in driving 2-line inversion (i.e., normally white mode that white presents when a power is not applied).

In the drawings, illustrated elements are a gate clock signal GATE CLOCK outputted from a timing control circuit 4, an output signal Vdrive of a source driving circuit in a conventional liquid crystal display, an output signal of a source driving circuit 3 in a liquid crystal display according to the present invention, and gate on signals GATE ON(n), GATE ON(n+1), GATE ON(n+2) and GATE On(n+3) that are outputted from the timing control circuit 4 in order to drive (n)th, (n+1)th, (n+2)th and (n+3)th lines.

The source driving circuit in the conventional liquid crystal display generates a liquid crystal driving voltage Vdrive having voltage level of V_{F+} and V_{F-} in each period of the gate clock GATE CLOCK. The voltage Vdrive is symmetric to positive and negative directions on the basis of a common voltage Vcom.

The source driving circuit 3 in the liquid crystal display 100 according to the

present invention generates a liquid crystal driving voltage Vdrive' = Vgray(t) that is changed by a gray voltage in each period of the gate clock signal GATE CLOCK. In each period of the gate clock signal GATE CLOCK, the voltage Vdrive' generates a liquid crystal driving voltage Vdrive' having different levels in high and low level intervals. That is, the liquid crystal driving voltage Vdrive' = Vgray'(t) generates positive and negative high voltage that are enough to rapidly charge liquid crystal capacitors Cp constructed in a liquid crystal panel 1. In this case, the liquid crystal driving voltage Vdrive' = Vgray'(t) generates the high voltages only for a predetermined interval, in order to prevent power consumption caused by generating such high voltages.

With reference to Fig. 8, in driving dot inversion, how to drive a positive polarity when applying a gate on signal Gate On(n) for driving an (n)th line, is now explained. If a gate clock signal Gate Clock is laid to high level, a source driving circuit 3 generates a liquid crystal driving voltage Vdrive' having first voltage level that is still higher than that of an existing liquid crystal driving voltage Vdrive. If Gate Clock is laid to low level, the source driving circuit 3 generates a liquid crystal driving voltage Vdrive' having a second voltage level of V_{F+} with the same polarity as Vdrive. In this case, both the first voltage level and the second voltage level are higher than a common voltage Vcom. And, the first voltage level is higher than the second voltage level.

When a gate-on signal Gate On(n) for driving an (n+1)th line is applied, driving a negative polarity is explained. If the gate clock signal Gate Clock is laid to high level, the source driving circuit 3 generates a liquid crystal driving voltage Vdrive' having third voltage level is still lower than that of the existing liquid crystal driving voltage Vdrive. If Gate Clock is laid to low level, the source driving circuit 3 generates a liquid crystal

driving voltage Vdrive' having fourth voltage level of V_{F-} with the same polarity as Vdrive. In this case, both values of the third voltage level and the fourth voltage level are lower than the common voltage Vcom And, the third voltage level is lower than the fourth voltage level.

With reference to Fig. 9, in driving 2-line inversion, when a gate on signal Gate On(n) for driving (n)th and (n+1)th lines is applied, driving a positive polarity is explained. If a gate clock signal Gate Clock is laid to high level, a source driving circuit 3 generates a liquid crystal driving voltage Vdrive' whose level is still higher than that of an existing liquid crystal driving voltage Vdrive. If Gate Clock is laid to low level, the source driving circuit 3 generates a liquid crystal driving voltage Vdrive' having voltage level of V_{F+} the same as Vdrive.

When a gate on signal Gate On(n) for driving (n+2)th and (n+3)th lines is applied, driving a negative polarity is explained. If the gate clock signal Gate Clock is laid to high level, the source driving circuit 3 generates a liquid crystal driving voltage Vdrive' whose level is still lower than that of the existing liquid crystal driving voltage Vdrive. If Gate Clock is laid to low level, the source driving circuit 3 generates a liquid crystal driving voltage Vdrive' of V_{F-} with the same polarity as Vdrive.

In Figs. 7 and 8, output waveforms of the source driving circuit 3 can be changed according to a kind of line driving methods, and are applicable to various kinds of line driving methods (e.g., n-line inversion driving method).

Figs. 10A, 10B, 11A, 11B; 12A, 12B, 13A and 13B show response speed measuring results of 0 through 32, 0 through 48, 0 through 64, and 32 through 84 gray levels of the source driving circuits by means of the gray voltage shown in Figs. 7A and

7B. In particular, Fig. 10A, Fig. 10B, Fig. 11A, and Fig. 11B show a response speed of 0 through 32 gray levels of a conventional source driving circuit, a response speed of 0 through 32 gray levels of a source driving circuit according to the invention, a response speed of 0 through 48 gray levels of the conventional source driving circuit, and a response speed of 0 through 48 gray levels of the source driving circuit according to the invention, respectively. Fig. 12A, Fig. 12B, Fig. 13A, and Fig. 13B show a response speed of 0 through 64 gray levels of the conventional source driving circuit, a response speed of 0 through 64 gray levels of the source driving speed according to the invention, a response speed of 32 through 64 gray levels of the conventional source driving circuit, and a response speed of 32 through 64 gray levels of the source driving circuit according to the invention, respectively.

The result can be obtained by measuring the 48-gray voltages ② and ②' and the 64-gray voltages ③ and ③' (see Figs. 7A and 7B) that were changed and applied with respect to five source driving circuits each having positive and negative polarities. A rising time of each waveform is denoted on the basis of a luminance, and corresponds to a falling time of a liquid crystal based on its movement.

Referring to Figs. 10A and 10B, in response speeds of a source driving circuit with respect to 0 through 32 gray levels, a conventional rising time (i.e., a falling time of a liquid crystal) is 26.0ms and a conventional falling time (i.e., a rising time of the liquid crystal) is 3.6ms. According to the present invention, a rising time (i.e., a falling time of a liquid crystal) is 24.2ms and a falling time (i.e., a rising time of the liquid crystal) is 3.6ms. In this case, a luminance-based falling time is not changed, while a luminance-based rising time is reduced from 26ms to 24.2ms by 1.8ms.

Referring to Figs. 11A and 11B, in response speeds of a source driving circuit with respect to 0 through 48 gray levels, a conventional rising time (i.e., a falling time of a liquid crystal) is 36.8ms and a conventional falling time (i.e., a falling time (i.e., a rising time of the liquid crystal) is 3.6ms. According to the invention, a rising time (i.e., a falling time of a liquid crystal) is 26.2ms and a falling time (i.e., a rising time of the liquid crystal) is 4.4ms. In this case, a luminance-based falling time increases in 0.8ms, while a luminance-based rising is reduced from 36.8ms to 26.2ms by 10.6ms.

Referring to Figs. 12A and12B, in response speeds of a source driving circuit with respect to 0 through 64 gray levels, a conventional rising time (i.e., a falling time of a liquid crystal) is 22.6ms, and a conventional falling time (i.e., a rising time of the liquid crystal) is 4.7ms. According to the invention, a rising time (i.e., a falling time of a liquid crystal) is 15.1ms, and a falling time (i.e., a rising time of the liquid crystal) is 4.6ms. In this case, a luminance-based falling time is reduced by 0.1ms, and a luminance-based rising time is reduced from 22.6ms to 15.1ms by 7.5ms.

Referring to Figs. 13A and 13B, in response speeds of 32 through 64 gray levels with respect to a source driving circuit, a conventional rising time (i.e., a falling time of a liquid crystal) is 20.8ms, and a falling time (i.e., a rising time of the liquid crystal) is 3.4ms. According to the invention, a rising time (i.e., a falling time of a liquid crystal) is 15.0ms, and a falling time (i.e., a rising time of the liquid crystal) is 3.4ms. In this case, a luminance-based falling time is not changed, and a luminance-based rising time is reduced from 20.8ms to 15.0ms by 5.8ms.

In Figs. 10A through 13B, response speeds of a source driving circuit 3 according to the present invention change as follows. In 0 through 32 gray levels, a

response speed is reduced from 26ms to 24.2ms by 1.8ms. In 0 through 48 gray levels, a response speed is reduced from 36.8ms to 26.2ms by 10.6ms. In 0 through 64 gray levels, a response speed is reduced from 22.6ms to 15.1ms by 7.5ms. And, in 32 through 64 gray levels, a response speed is reduced from 20.8ms to 15.0ms by 5.8ms. The following table [TABLE 1] represents these response speeds.

[TABLE 1]

Falling Times of Liquid Crystal		
	Prior Art	Present Invention
0-32 Gray Levels	26.0ms (1.00)	24.2ms (0.96)
0-48 Gray Levels	36.8ms (1.00)	26.2ms (0.71)
0-64 Gray Levels	22.6ms (1.00)	15.1ms (0.67)
32-64 Gray Levels	20.8ms (1.00)	15.0ms (0.72)

wherein these falling times are results of simulation that is carried out in the same condition, and numerals in parentheses denote normalized results on the basis of falling times of a conventional liquid crystal, respectively.

Referring to the normalized results in TABLE 1, in 0 through 32 gray levels, the falling time of the liquid crystal is improved by 7%. In 0 through 48 gray levels, the falling time is improved by 29%. In 0 through 64 gray levels, the falling time is improved by 33%. And, in 32 through 64 gray levels, the falling time is improved by 28%. In other words, the speed of the falling time of the liquid crystal is improved in proportion to the gray values.

As described above, a gray voltage generation circuit of this invention outputs an altered gray voltage Vgray' so that a source driving circuit can generate a liquid crystal driving voltage Vdrive' having a voltage level as shown in Figs. 7 and 8. Thus, the source driving circuit 3 generates a liquid crystal driving voltage Vdrive' = Vgray'(t) that changes according to a gray voltage in each period of a gate clock signal Gate Clock. Liquid crystal capacitors Cp constructed in a liquid crystal panel 1 are rapidly charged by the liquid crystal driving voltage Vdrive' applied from the source driving circuit 3. As a result, a falling time of the liquid crystal is reduced to improve a driving speed of a liquid crystal display.

While an illustrative embodiment of the present invention has been shown and described, numerous variations and alternate embodiments will occur to those skilled in the art, without departing from the spirit and scope of the invention. Accordingly, it is intended that the present invention not be limited solely to the specifically described illustrative embodiment. Various modifications are contemplated and can be made without departing from the spirit and scope of the invention as defined by the appended claims.